May 10, 1999

Silicon Subsystem Report

April 1999

Subsystem Manager's Summary (M. Gilchriese)

Cost and Schedule Summary Status

Milestones corresponding to the baseline schedule are marked with a *. Additional milestones are included, and will be included, as needed to monitor progress. Starting this month, we have changed the milestone reporting to better track changes each month. Baseline, previous-month and current milestones are reported.

1.1.1 Pixel System

Costs are within allocated limits. We have successfully increased our efforts on calculations and measurements in preparation for an Inner Detector cooling review at the end of May. Fundamental calculations were made of exhaust tube sizes for the baseline evaporative system, leading to modifications of the services layout. A sector prototype was tested at CERN with evaporative cooling up to power levels expected for "worst case" power dissipation(about 50% more than nominal) and results were good and similar to tests with water-based cooling at LBNL. A monophase(ie. liquid) fluorinert was purchased and used at LBNL to test a sector, since this is the back-up option to the evaporative system. The sector was cooled successfully and flow and other parameters were measured. The fabrication of the first prototype disk support ring started and is supported by SBIR funding. Work on the support frame prototype has started and a meeting at the fabricator was held to review material test results and design drawings. The design of the 2^{nd} prototype sensors is complete. Bids for fabrication of the 2^{nd} prototype sensors were received and evaluated. Two companies/consortia were selected and each will produce 20 wafers. Measurements after irradiation of prototype 1.5 sensors (these sensors include design modifications to prototype 1.0 sensors to eliminate small regions of poor efficiency at the pixel edges) are underway and test beam measurements will start in early May. The FE-D submission date continues to slide and is now projected for late June. To help this situation, an LBNL engineer will move to Bonn for a month to work on the final layout, integration, simulation and verification. There is now general agreement that we will have to provide additional funding to Temic and Honeywell to accelerate fabrication to recover some of the delays. A prototype analog chip made in the Honeywell SoI process was received and preliminary tests are very encouraging. It appears that this process is entirely acceptable for analog design. Additional measurements, including after irradiation will occur over the next two months. The basic design of the next prototype flex hybrid, 1.x, is complete. The basic design must be tweaked for each vendor and this has been done for fabrication at CERN and will be complete shortly for another vendor in the US(R&D Circuits in New Jersey). Fabrication with GE has been put on hold, since

their costs are higher and it appears that cheaper vendors can do the job. New 16-chip modules were received from IZM in Berlin. These were X-rayed to assess flip chip yield and to compare with X-rays done at IZM. We found discrepancies(more defects) and are working with IZM to resolve this. The modules were characterized at LBNL in preparation for test beam measurements in May. A flex module was also assembled at LBNL.

1.1.2 Silicon Strip System

Costs are within allocated limits. However, to accelerate the fabrication of the ABC and ABCD, a BCP will be submitted in May. Two CAFE-P wafers arrived from Maxim (a few days before the baseline date) and four more wafers are waiting at first metal in case we want to make last minute changes based on evaluation of the first two wafers. Preliminary tests indicate performance as expected from simulation. First irradiation tests will occur on May 6 at LBNL. The ABCD was submitted to Temic on April 8. Work on the ABC was completed at RAL on April 23 and the database moved to LBNL for final cross-checks, including some design rule checking that RAL cannot do and additional top-level verifications. The ABC was submitted from LBNL to Honeywell on May 1. The Frame Contract covering all rad-hard IC procurements was approved by the CERN finance committee in March and negotiations on final terms and conditions with the vendors is underway by CERN procurement with some involvement by us.

1.1.3 ReadOut Driver System

Costs are within allocated limits. Following the March 25-26 review that recommended an architecture using FPGAs in the data stream and DSPs for other tasks such as monitoring and calibration, design work focused on completing architectural studies. Work by Wisconsin concentrated on understanding the best use of the DSPs. Work by Irvine concentrated on requirements and tools for monitoring event data flow and on interfacing the DSPs. The schedule for the preprototype ROD must be rewritten to account for delays in finalizing the architectural design. As described last month, the delay encountered to date will not result in a delay to the SCT schedule because its need for SCT system tests has been delayed by other delays in SCT electronics development. Nonetheless, the architectural design work must be brought to completion in order to ensure that further delays do not impact either the SCT system tests or the schedule for the production RODs. Initiation of design work on the ROD test stand, which had been scheduled for April, has been deferred in favor of the ongoing architectural design work. The schedule for test stand design will be rearranged to maintain the original completion date. Support is ongoing for Pixel and SCT tests in laboratories and beams.

Detailed Reports

1.1.1 Pixel System

1.1.1.1 Mechanics (E. Anderssen, D. Bintinger, M. Gilchriese)

Milestones	Baseline	Previous	Current	Status
*ID Eng. Review at CERN	20-Oct-98	20-Oct-98		Done
Select prototype ring concept	1-Nov-98	1-Feb-99		Done
Select materials for frame proto.	15-Mar-99	7-Apr-99		Done
Complete fab 1st prototype ring	1-Apr-99	15-May-99	15-May-99	Delay
Complete frame Phase I	1-Jul-99	1-Jul-99	1-Jul-99	OK
Complete fab 1st prototype disk	1-Jul-99	1-Jul-99	1-Jul-99	OK
*Select sector baseline concept	1-Sep-99	1-Sep-99	1-Sep-99	OK
*Module attachment CDR	1-Sep-99	1-Sep-99	1-Sep-99	OK
*Compl test of 5-disk prototypes	1-Sep-99	1-Sep-99	1-Sep-99	OK
Complete frame Phase II	1-Oct-99	1-Oct-99	1-Oct-99	OK
Complete frame Phase III	1-Feb-00	1-Feb-00	1-Feb-00	OK

LBNL/CERN

1.1.1.1.1 Design

Calculations of system flow parameters for pixel cooling with evaporated C4F10 were made by Hytec, Inc. These parameters will aid in setting exhaust line sizes and will be compared to tests of evaporative cooling with C4F10 at CERN. Calculations of system flow parameters for pixel cooling with liquid C6F14 were made at LBNL. Cooling with liquid C6F14 is a backup system for evaporative cooling. These calculations are being made for a cooling review to be held at CERN on May 26-28.

The layout of the pixel services was modified to allow pipe diameters indicated by these calculations. The power cable layout was also revised to take into account "worst case" electronics dissipation based on a 400 micron pixel size in all but the B-layer.

A visit was made to the fabrication vendor(Allcomp) for the support frame prototype. Allcomp had produced a test laminate panel and the basic properties of this panel were measured and meet expectations. Additional panels will be manufactured and tested both by an external vendor and by LBNL. The latter will also irradiate samples and measure material properties after irradiation. Design drawings for the prototype frame panels were reviewed.

1.1.1.1.2 Development and Prototypes

TV Holography tests on aluminum tube sector 4 at Hytec, Inc to determine out-of-plane distortions as a function of pressure within the cooling tube indicated that the edges of the unsupported overhangs of the sector deformed approximately 1 micron per psi. The tests at Hytec were performed at room temperature. Tests performed at LBNL using an imaging CMM at room temperature and at -7 degrees C gave similar results. Also tests after aluminum tube sector 4 had been cycled to 60 psi 20 times indicated the same level of distortion per psi. Tests at LBNL to measured distortion of aluminum tube sector 4 as a function of temperature showed out-of-plane distortion at the edges of the overhangs of approximately 20 microns for a temperature change from +20 to -18 degrees C. All the above tests were performed without dummy silicon modules mounted to the sector.

TV Holography tests performed on silicon modules tacked with UV curing epoxy to carbon-carbon sector mockups indicated that the UV epoxy tacks caused no excessive distortion beyond that seen from the compliant thermal compound fixing the silicon to the carbon-carbon. The UV cure epoxy will aid in quickly fixing pixel modules to the support structures after precision placement.

Construction of the support ring for the first prototype disk has commenced.

A test of cooling with liquid C6F14 on aluminum tube sector 3 was performed at LBNL. Preliminary results indicate that C6F14 can cool pixel sectors with an inlet temperature of -20 degrees C and flow rates of 17 cc/sec for a power disipation of 9 Watts per module. Further tests will be conducted on staves supplied by Genoa.

1.1.1.1.3 Disk Production
No activity.

1.1.1.2 Pixel Sensors (S. Seidel)

Milestones	Baseline	Previous	Current	Status
*Start market survey	2-Nov-98	1-Dec-98		Done
*2nd prototype PDR	1-Dec-98	1-Dec-98		Done
*Complete market survey	5-Mar-99	12-Feb-99		Done
*2nd prototype FDR	29-Mar-99	22-Feb-99		Done
*Compl. Test 1st prototypes	13-Apr-99	13-Apr-99		Done
*Compl. 2nd prototype design	27-Apr-99	27-Apr-99		Done
*Compl. Fab of 2nd prototypes	21-Sep-99	30-Aug-99	21-Sep-99	OK

1.1.1.2.1 Design

Design of the Second Prototypes was completed.

1.1.1.2.2 Development and Prototypes

Two of the three manufacturers who responded to the Price Enquiry were qualified for fabrication of Second Prototypes. A decision was taken to order 20 wafers from each.

IV measurements were made at New Mexico on 4 Prototype 1b single-chip sensors and 3 Prototype 1c wafers (51 single chip sensors). Irradiated devices were studied at –20C to permit operation at high voltage. Although statistics are limited, it appears that "thin" wafers have poorer breakdown characteristics than 300 micron ones. Plots from the measurements can be found at http://wwwhep.phys.unm.edu/atlas_pixel/1_5_prototypes/. A compilation of the results is in progress.

1.1.1.2.3 Production

No activity.

1.1.1.3 Pixel Electronics (K. Einsweiler, R. Kass)

Milestones	Baseline	Previous	Current	Status
Compl. Design HSOI test die	16-Apr-98	1-Nov-98		Done
Compl. Fab HSOI test die	26-Aug-98	31-Mar-99		Done
Compl. Design DMILL test device	15-Dec-98	15-Dec-98		Done
Submit 2nd Honeywell SoI test die	15-Jan-99		Not known	
1st design review of DMILL proto	25-Jan-99	23-Feb-99		Done
*FDR DMILL 1st prototype	25-Jan-99	TBD	15-Jun-99	Delay
*Compl. Design DMILL 1st proto.	26-Feb-99	1-May-99	30-Jun-99	Delay
1st design review of Honey. Proto	1-Jun-99	1-Jun-99	1-Oct-99	Delay
Compl. Eval. HSOI test die	1-Jul-99	1-Jul-99	1-Aug-99	Delay
*FDR Honeywell SoI 1st prototype	5-Mar-99	15-Jul-99	15-Nov-99	Delay
*Compl. Design Honey. SoI proto.	2-Apr-99	1-Oct-99	1-Dec-99	Delay
*Compl. Fab of DMILL 1st proto.	23-Jul-99	7-Sep-99	15-Oct-99	Delay
*Compl. Fab of Honey. SoI 1st proto	25-Aug-99	15-Feb-00	1-Mar-00	Delay
*Compl eval. DMILL prototype	9-Dec-99	1-Jun-00	1-Jun-00	Delay
*Compl eval HSOI prototype	15-Feb-00	1-Jun-00	1-Jun-00	Delay
*Review design approach	19-Jan-00	15-Jun-00	15-Jun-00	Delay
*Select rad-hard vendor	29-Jan-00	15-Jul-00	15-Jul-00	Delay

The date for submission of a 2nd set of test die to Honeywell is not known at this time and this submission may not occur. The delay for the submission of the DMILL rad-hard prototypes (FE-D) continues to increase due to lack of critical manpower. This is on the critical path for the pixel sub-system. Submission of the Honeywell rad-hard prototypes (FE-H) is significantly delayed by comparison to our original schedule due to the decision to focus all resources on the DMILL submission first. These two critical milestones have slipped far enough that we will be willing to pay the vendors extra in order to get the shortest reasonable turn-around time (typically 8-12 weeks instead of the more usual 16-20 weeks). Pending approval by the collaboration, we will seek to negotiate the more aggressive turn-around times with both Temic and Honeywell.

1.1.1.3.1 Design
LBNL
Our highest priority remains the DMILL front-end chip submission (FE-D). We have worked to transfer design knowledge from our departing engineer (A. Joshi) to the remaining engineers on the project. Unfortunately, due to continued delays in the SCT ABC submission, one critical engineer remains unavailable.

The layout work for the digital readout portion of the chip is now almost completed, after recent revisions for buffer size increases required to meet timing specifications after irradiation. This effort has caused quite some delay as we realized that many details of the

layout work left by our departed engineer had not been properly simulated with corner models (worst case post-irradiation in particular). This has caused us to take some significant steps backwards, and to pass off more of the layout work to Bonn, as our continued critical engineering situation has not allowed us to complete our responsibilities in a timely manner. This work should be completed in the next 1-2 weeks, including the integration of the bottom of column region (between columns and end-of-column logic). This region is the most complex in the chip, including biassing circuitry for the analog front-end blocks, control circuitry for the columns, and arbitration, sense amplifier and buffer blocks for the digital readout. This integration work is taking place largely in Bonn. After this is complete, full-scale worst-case simulations will be done to resolve any remaining system-level performance issues in the complete column and end-of-column logic.

Our remaining steps for the submission are to finalize the readout sequencer that operates the digital readout of the chip, and to complete integration of the support circuitry at the bottom of the chip. Our lead engineer on FE-D will leave in two weeks to spend the following 4 weeks working on this final integration in Bonn. At this time, we hope to be very close to a final version of the complete chip.

We are still awaiting the responses from TEMIC to our list of technical questions. These are needed to finalize details of the submission, and to resolve remaining small issues with the reticle layout and the design rules, particularly the relationship between the “advice” rules and the expected yield.

Ohio State

The existing DORIC4 chip uses BICMOS technology with only NPN transistors to achieve a radiation tolerant design. We are developing a version of the DORIC4 chip using a radiation hard CMOS process (Honeywell SOI and/or DMILL). In consultation with the team that designed the DORIC4 we have put together a spice model of the chip which uses n-FETs and p-FETs.

We have simulated a complete version of the chip, excluding the LVDS drivers. This simulation includes a newly designed preamp and "delay control" amplifier (in the feedback loop). In the simulations both the 40 MHz clock and the encoded data are successfully generated. A series of simulations is underway to determine how sensitive the circuit is to variations in circuit element parameters (e.g. bias voltages and resistor values).

Future work includes adding drivers to the circuit and modeling the new circuit. Chuck Rush has been in contact with Michal Ziolkowski (Siegen) concerning the design, simulation and layout of the chip. A submission to DMILL is planned to occur with the FE-D submission.

1.1.1.3.2 Development and Prototypes

LBNL

We have been working for the last few weeks on detailed timing measurements using an IR laser test stand. These measurements have uncovered a small instability in the FE-B timing generation, in the Grey code generator that supplies the 7-bit timestamp used to establish the timing of all hits in the front-end chip. The source of this is not understood, but it seems that each time this generator is reset, the phase relationship between the input 40 MHz clock and the output timestamps can jump randomly by up to 1ns. This is not a fatal error, but we have not been able to isolate its cause. We have managed to largely work around this problem, and make some high quality measurements of timing in both single chip and module assemblies.

These measurements have shown a large dependence (up to 4ns peak) of the transit time through a pixel when the threshold is varied. This is most likely due to the particular biassing configuration of the discriminator, and suggests that a modified design would give less timing dispersion in a complete system, since not all threshold adjustments will be set to identical values. In addition, the expected pattern of relative timing within a chip has been measured. This largely confirms the delays expected from a simple R-C transmission line model of the two-dimensional timestamp distribution tree. These differing internal delays introduce an additional 1.5ns RMS timing jitter, compared to the raw jitter of a particular pixel (already measured to be well below 1ns). Finally, measurements on a complete module have also been made. In this case, the clock distribution was performed on the printed-circuit support card rather than on a real Flex, and so effects due to the layout needed to be measured empirically (using pico-probes) and subtracted out. The resulting time distribution suggested that chip-to-chip timing uniformity will not add significantly to the uniformity already measured within a single chip. However, due to the dependence on threshold setting, these measurements still require refinement.

The Honeywell SOI multi-project submission which we made in Nov. 98 has returned to LBL and undergone preliminary evaluation. First results are very encouraging, with only one modest layout error discovered so far (which only affects particular cross-coupling tests). The basic summary is that the HSOI front-end design works better than or as well as the front-end of FE-B. The preamplifier risetime is excellent, and the measured noise agrees well with that found in FE-B. The threshold dispersion appears to be significantly better than FE-B. This was qualitatively expected, but the magnitude of the improvement is larger than we can explain quantitatively at this time. The timewalk performance appears to be as good as, and probably somewhat better than, FE-B. These first results indicate that indeed this process can be used for analog front-ends in pixel chip design. Further characterization work will continue, including more detailed comparisons with the actual device parameters for this run, extracted from test structures. Finally, once we have several well-characterized devices, we will carry out irradiations in the LBL 88” cyclotron. The present devices, which were fabricated using a multi-project run with Honeywell, were not made using the “enhanced” version of the SOI process which we wish to use for ATLAS. They were fabricated using the standard process, which we have shown does have some problems with large threshold shifts in PMOS transistors after 25 MRad. Thus we do not expect to achieve the full dose performance for ATLAS, but we should be able

to scale from these results, and our knowledge of the devices in the enhanced process, to a good understanding of what to expect.

1.1.1.3.3 Production

No activity.

1.1.1.4 Pixel Hybrids (R. Boyd)

Milestones	Baseline	Previous	Current	Status
* Compl. Assembly of 1st proto.	14-Jan-99	10-Nov-98		Done
* 1st prototype design review	18-Feb-99	18-Feb-99		Done
* Compl. Tests of 1.0 protos.	15-Apr-99	15-Mar-99		Done
* Select hybrid type	15-Apr-99	1- Mar-99		Done
Compl. Design of 1.x proto		1 - Apr- 99	21-Apr-99	Done
Fabrication of 1.x compl			1-Aug-99	OK
Singulate 1.x proto compl			15-Aug-99	OK
Assembly of 1.x proto compl			1-Sep-99	OK
Prototype 1.x tests complete			15-Oct-99	OK
Module assy with 1.x compl			15-Sep-99	OK
Design of proto 2.0 begins			1-Sep-99	OK

Oklahoma
1.1.1.4.1 Design
A new schedule has been defined based on lessons learned from the version 1.0 Flex Hybrid prototypes module prototypes. This schedule is also more in line with the realities of the deliveries of other components including the FE-D, rad-hard MCC, first prototype Optical Links, bumped bare modules and the different design rules provided by various flex manufacturers. In addition, the increased number of prototypes allows for evaluation of more flex manufacturers, which should lead to reduced costs and higher quality for the production Flex Hybrids. The '.x' is a place holder which will be replaced by a number representing the manufacturer specific design.

The base design for the 1.x Flex Prototype has been completed (based on the CERN fabrication design rules). Design reviews in April have led to several iterations of the design as it is modified to match the design rules of more vendors and errors are corrected. Submission is expected in early May to CERN and R&D Circuits. Submission to GE is currently being reconsidered. Work is still under way to identify tasks to be performed in connection with Flex Hybrid development through next summer.
Components sent to LBNL for irradiation were returned in late March and are currently undergoing evaluation. Results will be available in May.
Attempts to build a second module at OU were thwarted by poor wire bonding on the flex hybrids. This problem is being discussed with CERN fabrication personnel in an attempt to understand the source of the difficulty.

The files and data required by Albany (below) will be made available upon vendor approval of the designs.

1.1.1.4.2 Development
Oklahoma
Simulations continue with Ansoft Maxwell Spicelink. Confidence in the simulations is being built by simulating progressively more complex structures and comparing them with analysis and measurements.

Albany

At Albany we continue towards making a setup to test the flex circuits on our probe station.

1) We have made timing measurements which indicate with our present technology (computer aided probes) it will take us 250 minutes to measure one flex.

2) We are discussing with vendors the feasibility of making probe cards to speed up the testing process significantly. Final design and prices of the probe card cannot be finalized until we get the numerical coordinate file of pad positions in the next version (1.x).

3) We are ready to order a new mounting jig for the ATLAS flex on our probe station, but we are waiting for the geometry file from Oklahoma.

1.1.1.4.3 Production
No activity.

1.1.1.5 Pixel Modules (R. Boyd, K. Einsweiler, K. K. Gan, M. Gilchriese)

Milestones	Baseline	Previous	Current	Status
*Compl. 1st proto. Design	29-Oct-98	1-Mar-99		Done
*1st proto. Design review	18-Feb-99	18-Feb-99		Done
*Compl. Tests of 1st protos.	18-Mar-99	17-Sep-99	17-Sep-99	Delay
*Select module type	18-Mar-99	22-Feb-99		Done
*2nd proto. Design review	17-Sep-99	10-Sep-99	10-Sep-99	OK

1st prototypes will continue to be tested during the May and July test beam cycles.

1.1.1.5.1 Design/Engineering.

No activity.

1.1.1.5.2 Development and Prototypes

LBNL

We have received the single chip and module assemblies that are to be tested in H8 in mid-May. The single chip devices have been mounted and characterized. One device is defective due to the bumping vendor choosing a known bad die from the electronics wafer. The other assemblies are still under study, and we expect them to be ready for travel to Geneva by May 9. These devices are all based on the new sensor design known as prototype 1.5, and include a mixture of sensor designs that are either 280μ and 200μ thick. Due to delays in the Flex 1.x production, we have decided to use the recent modules to continue testing the Flex 1.0 design, and we hope to complete fabrication and assembly of a new such module by May 8, which could then be tested in the May H8 testbeam. We are also completing upgrades of the testbeam DAQ software to support acquisition from a complete module of 16 chips and a module controller chip (MCC). Previous testbeam operation never read out more than a single chip at any given time. This work should be complete in the next few days, and will be debugged during intial testbeam operation in one week.

Two 16-chip modules and four single-chip assembles made by IZM were X-rayed to determine the flip-chip yield. IZM had previously done X-rays. Our results indicate about a factor of two worse defect rate than measured by IZM. Our detailed results and pictures were transmitted to IZM and we are working with them to understand the discrepancies.

Ohio State

We have successfully produced a three dimensional mask for depositing wire bonding traces on the base of the optical package. To reduce drill breakage, the mask was made of brass instead of stainless steel and larger drill was used, producing 175 microns wide slit on the mask instead of 100 microns designed. The mask needs to be further refined in the future because the wider traces (slit) reduce the spacing between traces, increasing the possibility of shorts. Using the produced mask, Au/Cr traces were successfully deposited on the base with good electrical continuity over the 90^0 bend, proving the principle of three dimensional trace deposition. The traces were wire bondable. It is difficult to mount the tiny VSCEL's (250 microns x 250 microns) on the base and the tension in the wire bond sometimes lift the glued chip off the base. We are investigating alternative method of mounting the chips. Jigs for wire bonding and fibre placement have been successfully tested. We are also able to modify the fibre cleaver to strip 1.2 mm of cladding off the fibre instead of 6 mm as designed by the manufacturer. Two optical packages each containing 2 VSCEL's were fabricated and shipped to Oxford University for testing. The Oxford group was able to detect an optical signal but the power was weak because there is considerable slop in the placement of the cap with respect to the base. This is not too surprising because we concentrated on producing a package without strong emphasis on precision machining as a proof of principle. In the near future, the emphasis is on precise machining of the base and cap for better alignment to improve the optical power coupling.

1.1.1.5.3 Production

No activity.

1.1.2 Silicon Strips

1.1.2.1 IC Electronics (A.A. Grillo)

Milestones	Baseline	Previous	Current	Status
*Send out market survey	1-Sep-98	17-Aug-98	17-Aug-98	Done
*FDR for 2nd CAFÉ-M	15-Sep-98	11-Sep-98	11-Sep-98	Done
*Procurement in place for 2nd proto	9-Oct-98	13-Nov-98	13-Nov-98	Done
*FDR for 2nd ABC	23-Oct-98	26-Jan-99	26-Jan-99	Done
*Closing date for market survey	26-Oct-98	25-Sep-98	25-Sep-98	Done
*Submit 2nd CAFÉ-M	30-Oct-98	26-Jan-99	26-Jan-99	Done
*Issue call for tender	9-Nov-98	9-Nov-98	9-Nov-98	Done
*Submit 2nd ABC	16-Nov-98	30-Apr-99	1-May-99	Done
*FDR for 2nd ABCD	11-Dec-98	15-Dec-99	15-Dec-99	Done
*Closing date for tender	21-Dec-98	22-Jan-99	22-Jan-99	Done
*Submit 2nd ABCD	27-Jan-99	15-Apr-99	8-Apr-99	Done
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	15-Mar-99	Done
*Frame contract in place	15-Apr-99	15-Apr-99	30-May-99	Delay
*Compl. Fab of 2nd CAFÉ-M	19-Apr-99	16-Jun-99	8-Apr-99	Done
*Compl. Fab of 2nd ABC	19-Apr-99	15-Sep-99	13-Sep-99	Delay
*Test systems complete	26-Apr-99	31-Jul-99	31-Jul-99	Delay
*1st ICs avail. For 2nd proto hybrid	18-May-99	30-Sep-99	30-Sep-99	Delay
*Compl. Fab of 2nd ABCD	30-Jun-99	31-Aug-99	23-Jul-99	Delay

1.1.2.1.1 Design/Engineering

LBNL & UCSC

Final checks of the ABCD were completed in early April and the design was submitted to Temic on 8-April. It still required the full month of April to complete the work on ABC. Some improvements were made in the power bussing. Extraction of the full netlist with parasitics and final top level Verilog simulations with back annotation were completed. RAL completed its work on 23-Apr at which time the data base was moved to LBNL for final cross-checks. This included further Design Rule Checks that RAL did not have the capability to run and more top level Verilog simulations using a different set of test vectors. These tests were completed during the last week of April and the design was submitted to Honeywell on Saturday 1-May.

1.1.2.1.2 Development and Prototypes

LBNL & UCSC

Maxim surprised us this month by shipping the first two CAFÉ-P wafers two months early. Apparently, someone in their production control incorrectly tagged the lot as high priority. We received two of the six wafers ordered with four more waiting at first metal in case we want to make a last minute change after testing the first two. Two dice were looked at briefly with the old CAFÉ-M probe card and found to be functional. At that point roughly 20% of that wafer was cut so that more detailed tests could be performed. Results are still very preliminary but all tests so far show performance as expected from simulations. We will try to irradiate a few chips as soon as possible to confirm that the fix for post-irradiation channel matching worked.

Unfortunately, no one at Temic nor Honeywell is likely to incorrectly tag the ABCD or ABC lots as high priority, at least not for free. However, we are negotiating with both vendors to accelerate the fabrication process. Any decrease in fab time will be welcome given that our program is behind schedule. If we can receive the wafers at the end of July or early August, there is a small chance we can get some new chips built into modules for the September beam tests at CERN. Temic has offered to accelerate the fabrication process if the collaboration is willing to pay a premium of 18 kCHF. Honeywell has proposed a similar speed-up for $15k but they have not yet secured the agreement of their fabrication manager. We plan to accept the Temic offer and also the Honeywell one if we can get buy-in of their production people.

1.1.2.1.3 Production

The Frame Contract was approved by the CERN Finance Committee in March and so CERN Purchasing is authorized to finish the final negotiations of terms and conditions with the vendors. That is proceeding and should be completed soon.

1.1.2.2 Silicon Strip Hybrids (C. Haber)

Milestones	Baseline	Previous	Current	Status
Complete design of 1st prototype	17-Nov-97	17-Nov-97		Done
Complete fab of 1st prototype	2-Feb-98	23-Mar-98		Done
Preliminary design review	3-Aug-98	1-May-99	TBD	Delay
*Compl. 2nd proto subs. design	29-Oct-98	15-May-99	1-May-99	Delay
*Compl. 2nd proto cable design	29-Oct-98	15-May-99	1-May-99	Delay
*Compl. 2nd proto fanout design	29-Oct-98	15-May-99	1-May-99	Delay
*Compl fab of 2nd proto substrate	11-Mar-99	1-Aug-99	15-Jul-99	Delay
*Compl fab of 2nd proto cable	11-Mar-99	1-Aug-99	15-Jul-99	Delay
*Compl fab of 2nd proto fanout	11-Mar-99	1-Aug-99	15-Jul-99	Delay
*Compl procure of 2nd proto comps	11-Mar-99	1-Aug-99	1-Jun-99	Delay
*Compl. 2nd proto assembly	17-May-99	15-Aug-99	15-Aug-99	Delay
*1st 2nd proto hybrids available	14-Jun-99	1-Sep-99	10-Jul-99	Delay

LBNL
1.1.2.2.1 Design

A final design review was held of the ABC chip last month. Among the results of that review were plans to all a new Vdd pad and to change the configuration on the ID4 line. Both of these have implications for the hybrids. This month we finally received a new layout of the ABC chip. The new coordinates were checked and new reference drawings of the chip for the hybrid layout work were produced. The hybrid CAD draftsperson was given a set of changes to make to the layout in order to make it compatible with the new ABC chip. These modifications are now underway and should be complete early next month. A new schematic was prepared and distributed. This was also reviewed with the group from Santa Cruz.

1.1.2.2.2 Development and prototype fabrication

Further discussions were held with the fabrication vendors in preparation for the next printing run. There were some questions about the final diced dimensions of the ABC. The old chip was measured as a way to determine the likely edge material excess.

It was decided to build 19 (5) thin (thick) hybrids at the standard vendor and 10(4) with the silver process.

1.1.2.2.3 Production

No activity.

1.1.2.3 Modules for Silicon Strips(C. Haber)

Milestones	Baseline	Previous	Current	Status
*Preliminary design review	3-Aug-98	1-Apr-99	T BD	Delay
Complete fabrication of 1st dummy modules	15-Aug-98	15-Aug-98		Done
Prototype tooling complete	1-Apr-99	1-Aug-99	1-Aug-99	Delay
*Compl. Design of proto assy/test	14-Jun-99	15-Nov-99	15-Nov-99	Delay
*Compl. Fab of tooling for proto	14-Jun-99	15-Nov-99	15-Nov-99	Delay

As noted below the tooling workshop will be held in late May. The module construction and evaluation activity is hostage, in part, to the lack of good front end ASICs. The delay indicated above reflects the slip in the time of the tooling workshop as well as the requirement to have built prototype modules with chips from the next submission. The 1-Aug-99 date for the completion of prototype tooling describes tooling which will have been tested only on dummy modules. The 15-Nov-99 date refers to electrically working modules.

LBNL
1.1.2.3.1 Design of Assembly and Test

A new version of the assembly software from Manchester is available and we are still studying the documentation.

1.1.2.3.2 Development and prototypes

A tooling workshop will be held at the Rutherford Lab in the UK the week of May 24, 1999. This was originally planned for March of 1999.

Design of a new calibration plate was completed in January 1999. Work began to prepare the GDS-2 file needed for fabrication in February and a GDS-2 file was completed last month. In the process we discovered an inconsistency in the detector spacing within the module among various "official" module drawings and specifications. This spacing is written into the plate so we must be sure it is correct and consistent with the errors expected in the wafer dicing. A detailed message was sent to all the people involved. This month we received a consensus opinion on how to handle the spacing issue that we will follow.

Design continued on a folding fixture for the hybrids.

The process of training a new technician on the assembly system continues. This individual is expected to be the lead technician on the module assembly during the construction phase.

The plan is to build a thermal test hybrid. We placed and order for the BeO sheets needed for the facings. We attempted to cut a sheet of PG for use in the baseboard but were not successful. We have contacted the experienced people in Europe but await a response.

We have located and procured a set of lubricants needed to maintain the module assembly system.

1.1.2.3.3 Production

No activity.

1.1.3 ReadOut Drivers(A. Lankford,R. Jared)

Milestones	Baseline	Previous	Current	Status
*Select PreROD implementation	30-Oct-98	26-Mar-99		Done
*Requirements review	30-Nov-98	18-Nov-98		Done
*Compl. System design	28-Dec-98	TBD	TBD	TBD
*System design review	11-Jan-99	TBD	TBD	TBD
*Compl. PreROD design	29-Jan-99	TBD	TBD	TBD
*Compl. PreROD layout	15-Feb-99	TBD	TBD	TBD
*Compl. PreROD procure	1-Mar-99	TBD	TBD	TBD

*Compl. PreROD PCB fab	16-Mar-99	TBD	TBD	TBD
*Compl. PreROD 1st assemble	30-Mar-99	TBD	TBD	TBD
*Compl. Test stand requirements	14-Apr-99	14-Apr-99	TBD	TBD
*Compl. Test stand essential mod.	12-May-99	12-May-99	TBD	TBD
*Compl. Test stand impl. Model	10-Jun-99	10-Jun-99	TBD	TBD
*Compl. PreROD assembly	9-Jul-99	TBD	TBD	TBD
*PreRODs complete	20-Aug-99	TBD	TBD	TBD
*Test stand design review	21-Sep-99	21-Sep-99	21-Sep-99	OK
*Compl. Design of test stand	28-Sep-99	28-Sep-99	28-Sep-99	OK
*LVL2/ROB interfaces compl.	1-Oct-99	1-Oct-99	1-Oct-99	OK
*ROD Common design PDR	1-Oct-99	1-Oct-99	1-Oct-99	OK
*ROD strip design PDR	1-Oct-99	1-Oct-99	1-Oct-99	OK
*ROD pixel design PDR	1-Oct-99	1-Oct-99	1-Oct-99	OK

1.1.3.1.1 Strip Test Beam Support (A. Lankford)

UC Irvine

Hardware and software support for laboratory and beam tests of SCT electronics and modules continued. Some additional ABC GALs were sent to users in Melbourne for an additional DSP readout system that was assembled.

1.1.3.1.2 Pixel Test Beam Support (R. Jared)

University of Wisconsin/LBNL

Hardware was debugged and VHDL code was written in April. The hardware effort was to continue the debugging of the PLL. The hardware defect was associated with the VME interface. It is not known why the chips were defective. Replacement of the chips resulted in operational cards. As of this time there are 15 operational cards and two cards that need to be tested. The code support was to implement the trigger delay FIFO. This addition gives the PLL the ability to issue multiple triggers at 40 MHz with arbitrary time intervals between triggers. The code has been written debugged and is now being incorporated into the DAQ software.

The PLL has been fundamental to testing of the pixel front-end chips and modules. Many institutions are using the cards. This is evident in the distribution of the PLLs that is listed below:

2 ea. LBNL	1 ea. Oklahoma
1 ea. Dormund	1 ea. Bonn
1 ea. New Mexico	1 ea. Marseille
1 ea. Udine	2 ea. Genova
1 ea. Milan	1 ea. Wuppertal
1 ea. KEK	

2 ea. at LBNL for distribution to Ohio and CERN

2 ea. at LBNL are being tested.

1.1.3.2.1 ROD Requirements

UC Irvine (A. Lankford)

Work to clarify requirement V.A.1.n.3 *Some capability to monitor data flow* was initiated. The intent is to make this requirement more specific by replacing or augmenting the set of sample capabilities by specification of required capabilities. For instance, the committee at the recent ROD review suggested the ability to access *S*-link status, buffer occupancy information, front-end status, *etc*. This requirement should be firmed up before completion of the implementation model in order to ensure that a design based upon the implementation model is capable of providing the needed functionality.

University of Wisconsin (R. Jared)

It has become clear that there will be a need to revisit the requirements in light of discussions with the strip and pixel communities. Specifically there may be a need to throttle individual links based on the front end occupancy, configuration commands may need to be issued during the periodic reset (about once a second), and pixels may require two fiber links per module. These and other emerging requirements will be addressed in the future.

1.1.3.2.2 ROD Essential Model

UC Irvine and University of Wisconsin (A. Lankford)

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No refinements of the essential model were made during April.

1.1.3.2.3 ROD Implementation Model

UC Irvine (A. Lankford)

Possible improvements to the architecture recommended by the recent ROD review committee were investigated. Technical feasibility of these solutions is being reviewed. This work emphasized tools for monitoring event data flow and interfacing the DSPs to the data stream, other ROD components, and VME. Work continued on a ROD software development platform using two cooperating TI DSP evaluation modules.

University of Wisconsin (R. Jared)

The March 25-26 ROD review selected a FPGA implementation with back end DSPs for calibration. Much work has been performed to understand the best use of the DSPs. Initial findings find that the DSPs can be used for control during calibration (one DSP controlling configuration and commands to the front-end chip and others performing analysis of calibration data) and one DSP used to

monitor errors and corrections. In all cases the main data path latency and bandwidth is not effected by the DSPs.

1.1.3.3.7 Preprototype ROD

The implementation model for the preprototype ROD is being developed in tandem with the model for the production ROD. Progress on the implementation model is discussed primarily above under WBS 1.1.3.2.3.

UC Irvine (A. Lankford)

Some design issues that are independent of the final architectural details of the ROD architecture were studied. Clock circuitry was designed. Power supply circuitry was studied. Some aspects of ball grid array (BGA) layout issues were investigated. Some design tools were studied.

University of Wisconsin (R. Jared)

Behavioral and VHDL simulation of the FPGA continue. The pixels RODs are being added to the simulation. This activity will take a few months to complete.